WHAT IS CLAIMED IS:

1. A semiconductor chip package comprising:

a first semiconductor chip on whose surface an electrode for wiring is formed; and

a second semiconductor chip on whose surface an electrode for wiring is formed, and which is integrated and mounted with the first semiconductor chip,

wherein the first semiconductor chip and the second semiconductor chip are integrated and mounted with respective reverse surfaces of the first semiconductor chip and the second semiconductor chip opposing one another.

2. A semiconductor chip package according to claim 1, further comprising:

an interposer in which a through hole is formed at a position corresponding to the electrode for wiring on the second semiconductor chip,

wherein the second semiconductor chip is fixed to a surface of the interposer at a portion of the surface of the second semiconductor chip, and the reverse surface of the first semiconductor chip is fixed to the reverse surface of the second semiconductor chip, and

the electrode for wiring on the second semiconductor chip is exposed at a reverse surface side of the interposer via the through hole.

3. A semiconductor chip package according to claim 1, further comprising:

an interposer in which is formed a through hole which is larger than

chip sizes of the first semiconductor chip and the second semiconductor chip; and

an adhesive sheet which is a sheet-shaped adhesive material provided on a surface of the interposer so as to cover the through hole,

wherein the reverse surface of the second semiconductor chip is fixed to a reverse surface of the adhesive sheet which is exposed via the through hole at an interposer reverse surface side, and the reverse surface of the first semiconductor chip is fixed to a surface of the adhesive sheet so as to oppose the reverse surface of the second semiconductor chip at a position at which the second semiconductor chip is fixed.

4. A semiconductor chip package according to claim 1, further comprising:

an interposer in which is formed a through hole which is smaller than a chip size of the first semiconductor chip and larger than a chip size of the second semiconductor chip,

wherein the first semiconductor chip is fixed to a surface of the interposer at a portion of the reverse surface of the first semiconductor chip, such that the through hole is covered, and

the reverse surface of the second semiconductor chip is fixed to the reverse surface of the first semiconductor chip which is exposed at a reverse surface side of the interposer via the through hole.

5. A semiconductor chip package according to claim 2, wherein the interposer has, at a reverse surface side thereof, a region which is sunken-in, and the through hole is provided at the sunken-in region.

6. A semiconductor chip package according to claim 3, wherein the interposer has, at a reverse surface side thereof, a region which is sunken-in, and the through hole is provided at the sunken-in region.

7. A semiconductor chip package according to claim 4, wherein the interposer has, at a reverse surface side thereof, a region which is sunken-in, and the through hole is provided at the sunken-in region.

8. A semiconductor chip package according to claim 1, further comprising:

an interposer in which a through hole is formed at a position corresponding to the electrode for wiring on the second semiconductor chip; and

an adhesive sheet which is a sheet-shaped adhesive material larger than a chip size of the second semiconductor chip, and which is provided at a surface of interposer so as to cover the through hole, and in which a hole smaller than the chip size of the second semiconductor chip is formed,

wherein the second semiconductor chip is fixed, at a portion of the surface thereof, to a surface of the interposer via the adhesive sheet,

the reverse surface of the first semiconductor chip is fixed to the reverse surface of the second semiconductor chip, and

the electrode for wiring on the second semiconductor chip is exposed at a reverse surface side of the interposer via the small hole of the adhesive sheet and the through hole.

9. A semiconductor chip package according to claim 2, wherein the interposer is formed of one of tape and a glass epoxy material.

10. A semiconductor chip package according to claim 3, wherein the interposer is formed of one of tape and a glass epoxy material.

11. A semiconductor chip package according to claim 4, wherein the interposer is formed of one of tape and a glass epoxy material.

12. A semiconductor chip package according to claim 8, wherein the interposer is formed of one of tape and a glass epoxy material.

13. A semiconductor chip package according to claim 3, wherein both surfaces of the adhesive sheet become viscous when heated.

14. A semiconductor chip package according to claim 8, wherein both surfaces of the adhesive sheet become viscous when heated.